Curriculum Vitae

Personal Data

Daniel A. Jiménez
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Citizenship

United States of America

Education

2002 Ph.D. Computer Sciences, The University of Texas at Austin
Thesis title: *Delay-Sensitive Branch Predictors for Future Technologies*

1994 M.S. Computer Science, The University of Texas at San Antonio
Thesis title: *Methods for Satisfying Hard Boolean Formulas*

1992 B.S. Computer Science and Systems Design, The University of Texas at San Antonio

Research Interests

Computer architecture; characterizing and exploiting the predictability of programs, cache management.

Compilers; low-level code-improving transformations such as code-reordering for improving instruction fetch bandwidth.

Employment History

9/1/2015–present Professor. Department of Computer Science and Engineering, Texas A&M University.

1/1/2013–8/31/2015 Associate Professor. Department of Computer Science and Engineering, Texas A&M University.

2012 Professor. Department of Computer Science, The University of Texas at San Antonio

2011-2012 Department Chair. Department of Computer Science, The University of Texas at San Antonio

2011–2012 Director. Center for High Performance Computing and Software, The University of Texas at San Antonio.

2007–2012 Associate Professor. Department of Computer Science, The University of Texas at San Antonio.

2010–2011 Visiting Research Faculty. Barcelona Supercomputing Center.

2008–2009 Associate Professor. Department of Computer Science, Rutgers University

2002–2008 Assistant Professor. Department of Computer Science, Rutgers University

2005 Visiting Research Faculty. Department of Computer Architecture, Technical University of Catalonia (UPC), Barcelona, Spain.

1999–2001 Research Assistant. Department of Computer Sciences, The University of Texas at Austin, under Prof. Calvin Lin.

1996–1999 Instructor/Research. Department of Rehabilitation Medicine, The University of Texas Health Science Center at San Antonio.

1996–1998 Instructor. Division of Computer Science, The University of Texas at San Antonio.

1995,1999 Teaching Assistant. Department of Computer Sciences, The University of Texas at Austin.

1994–1995 Programmer/Analyst. Department of Rehabilitation Medicine, The University of Texas Health Science Center at San Antonio.

1992–1994 Teaching Assistant. Division of Mathematics, Computer Science, and Statistics, The University of Texas at San Antonio.

1993 Research Assistant. Division of Mathematics, Computer Science, and Statistics, The University of Texas at San Antonio, under Prof. Rajendra V. Boppana.

Occasional consultant for Samsung.

Awards, Honors, and Impact

2017 Member of the "MICRO Hall of Fame" of authors who have published at least eight papers in the MICRO conference.

2016 Samsung's Exynos-M1 processor uses a "neural net branch predictor." – from *Samsung's Exynos-M1 CPU*, Hot Chips 2016. Jiménez worked with Samsung's team in Austin to design the branch prediction algorithm used in the Exynos-M1.

2015 Member of the "HPCA Hall of Fame" of authors who have published at least six papers in the HPCA conference. (As of 2017 the the requirement has moved to eight papers; Jiménez still qualifies with eight papers.)

2012 Computer Architecture Letters paper selected to be presented in the "Best of CAL Session" at HPCA 2012.

2011 Neural branch predictors inspired by Jiménez's research are documented to be implemented in current microprocessors including the AMD "Fusion" C-series and E-series APUs and the Oracle SPARC T4. Quotes from industry literature:

> "One particularly interesting feature is the **Neural Net Logic Branch Predictor**, which is designed to improve the ability of Series C and Series E APUs to deliver performance for today's workloads." – from *APU 101: All about AMD Fusion Accelerated Processing Units*, emphasis added
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> "The SPARC T4 processor incorporates new features such as Out-Of-Order (OOO) execution of instructions, **branch prediction using a simple neural net algorithm**, cryptographic processing integrated directly within the instruction pipeline with user-level access, and longer pipelines that enable a higher clock rate." – from *Overview and Frequently Asked Questions Oracle SPARC T4-4*, emphasis added
>
> The SPARC T4 has "**Perceptron branch prediction** (neural net / AI -vs- heuristic)" – from *Oracle PartnerNetwork Day – Satellite Event Italia, 31 Gennaio Extreme Performance: SPARC T4 & Supercluster*, emphasis added

2009 MICRO paper received IEEE "Top Pick from Computer Architecture Conferences" award.

2013–present IEEE Senior Member

2012–present ACM Distinguished Scientist

2009–present ACM Senior Member

2008–2015 ACM Distinguished Speaker

2006-2011 NSF CAREER award

2001–2002	Intel Foundation Graduate Fellowship, The University of Texas at Austin
1999	TA Service Commendation, Department of Computer Sciences, The University of Texas at Austin
1990–1992	Research Careers for Minority Scholars Scholarship, The University of Texas at San Antonio

*In the following publications, * marks student authors supervised by Jiménez.*

Refereed Conference Papers

Daniel A. Jiménez, Elvira Teran*, *Multiperspective Reuse Prediction*, Proceedings of the 50th ACM/IEEE International Symposium on Microarchitecture (MICRO-50), Boston, MA October 2017. Acceptance rate: 18%.

Jinchun Kim, Elvira Teran*, Paul V. Gratz, Daniel A. Jiménez, Seth H. Pugsley, and Chris Wilkerson, *Kill the Program Counter: Reconstructing Program Behavior at the Last Level Cache*, Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2017), Xi'an, China, April 2017. Acceptance rate: 17.4%.

Zhe Wang*, Daniel A. Jiménez, Tao Zhang, Gabriel Loh, Yuan Xie, *Building a Low Latency, Highly Associative DRAM Cache with the Buffered Way Predictor*, The 28th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2016), Los Angeles, California, October 2016. Acceptance rate: 35%.

Elvira Teran*, Zhe Wang*, Daniel A. Jiménez, *Perceptron Learning for Reuse Prediction*, Proceedings of the 49th ACM/IEEE International Symposium on Microarchitecture (MICRO-49), Taipei, Taiwan, October 2016. Acceptance rate: 22%.

Elvira Teran*, Yingying Tian*, Zhe Wang*, Daniel A. Jiménez, *Minimal Disturbance Placement and Promotion*, Proceedings of the 22nd International Symposium on High Performance Computer Architecture (HPCA-22), pp. 201 – 211, Barcelona, Catalunya, March 2016, Acceptance rate: 22%.

David Kadjo, Jinchun Kim, Prabal Sharma, Reena Panda, Paul Gratz, and Daniel A. Jiménez, *B-Fetch: Branch Prediction Directed Prefetching for Chip-Multiprocessors*, Proceedings of the 47th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-47), Cambridge, UK, December 2014. Acceptance rate: 19%.

Yingying Tian*, Samira Khan*, Daniel A. Jiménez, and Gabriel Loh, *Last-Level Cache Deduplication*, Proceedings of the 2014 International Conference on Supercomputing (ICS 2014), Munich, Germany, June 2014. Acceptance rate: 21%.

Zhe Wang*, Daniel A. Jiménez, Cong Xu, Guangyu Sun, Yuan Xie, *Adaptive Placement and Migration Policy for an STT-RAM-Based Hybrid Cache*, Proceedings of the 20th International Symposium on High Performance Computer Architecture (HPCA-20), Orlando, Florida, February 2014. Acceptance rate: 25%.

Samira Khan*, Alaa R. Alameldeen, Chris Wilkerson, Onur Mutlu, Daniel A. Jiménez, *Improving Cache Performance Using Read-Write Partitioning*, Proceedings of the 20th International Symposium on High Performance Computer Architecture (HPCA-20), Orlando, Florida, February 2014. Acceptance rate: 25%. **Nominated for Best Paper at HPCA.**

Daniel A. Jiménez, *Insertion and Promotion for Tree-Based PseudoLRU Last-Level Caches*, Proceedings of the 46th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-46), Davis, California, December 2013. Acceptance rate: 16%.

Samira Khan*, Alaa Alameldeen, Chris Wilkerson, Jaydeep Kulkarni and Daniel A. Jiménez, *Improving Multi-Core Performance Using Mixed-Cell Cache Architecture*, 19th International Symposium on High Performance Computer Architecture (HPCA-19), Shenzhen, China, February 2013. Acceptance rate: 20%.

Zhe Wang*, Samira M. Khan*, Daniel A. Jiménez, *Improving Writeback Efficiency with Decoupled Last Write Prediction*, Proceedings of the 39th International Symposium on Computer Architecture (ISCA), Portland, Oregon, June 2012. Acceptance rate: 18%.

Samira M. Khan*, Zhe Wang*, Daniel A. Jiménez, *Decoupled Dynamic Cache Segmentation*, Proceedings of the 18th International Symposium on High Performance Computer Architecture (HPCA-18), February, 2012, pp 1 - 12. Acceptance rate: 17%.

Zhe Wang*, Daniel A. Jiménez, *Program Interferometry* Proceedings of the 2011 International IEEE International Symposium on Workload Characterization (IISWC), pp. 172–183, Austin, Texas, November 2011.

Daniel A. Jiménez, *An Optimized Scaled Neural Branch Predictor*, Proceedings of the 2011 IEEE International Conference on Computer Design (ICCD), Amherst, Massachusetts, October 2011. Acceptance rate: 28%.

Zhe Wang*, Daniel A. Jiménez, *Program Interferometry* (**poster and abstract**), Proceedings of the 2011 International Conference on Parallel Architectures and Compilation Technologies (PACT), Galveston, Texas, October 2011. Acceptance rate: 25% ((35 regular papers + 21 posters+abstracts) / 221 submissions).

Hyungjun Kim, Pritha Ghoshal, Boris Grot, Paul V. Gratz, Daniel A. Jiménez, *Reducing Network-on-Chip Energy Consumption Through Spatial Locality Speculation*, Proceedings of the Fifth ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2011), Pittsburgh, Pennsylvania, May 1-4, 2011. Acceptance rate: 25%.

Samira M. Khan*, Yingying Tian*, Daniel A. Jiménez, *Sampling Dead Block Prediction for Last-level Caches*, Proceedings of the 43rd International Symposium on Microarchitecture (MICRO-43), Atlanta, Georgia, December 2010. Acceptance rate: 18%.

Samira M. Khan*, Daniel A. Jiménez, *Insertion Policy Selection Using Decision Tree Analysis*, Proceedings of the 2010 IEEE International Conference on Computer Design (ICCD), Amsterdam, Netherlands, October 3–6, 2010. Acceptance rate: 30%.

Samira M. Khan*, Daniel A. Jiménez, Doug Burger and Babak Falsafi, *Using Dead Blocks as a Virtual Victim Cache*, Proceedings of the 2010 International Conference on Parallel Architectures and Compilation Technologies (PACT), Vienna, Austria, September 11–15, 2010. Acceptance rate: 17%.

Daniel A. Jiménez, *Composite Confidence Estimators for Enhanced Speculation Control*, Proceedings of the 21st International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2009), São Paulo, Brazil, pp. 161–168, October, 2009. Acceptance rate: 35%.

Renée St. Amant, Daniel A. Jiménez, and Doug Burger, *Low-Power, High-Performance Analog Neural Branch Prediction*, Proceedings of the 41st International Symposium on Microarchitecture (MICRO-41), Lake Como, Italy, pp. 447-458, November 2008. Acceptance rate: 19%.

Miquel Pericàs, Adrian Cristal, Ruben González, Daniel A. Jiménez, Alex Veidenbaum, and Mateo Valero, *A Two-Level Load/Store Queue Based on Execution Locality*, Proceedings of the 35th International Symposium on Computer Architecture (ISCA), Beijing, China, pp. 25–36, June 2008. Acceptance rate: 14%.

Miquel Pericàs, Adrian Cristal, Ruben González, Daniel A. Jiménez, and Mateo Valero, *A Flexible Heterogeneous Multi-Core Architecture*, Proceedings of the International Conference on Parallel Architectures and Compilation Technologies (PACT), Braslov, Romania, pp. 13–24, September 2007. Acceptance rate: 19%.

Chunling Hu*, Daniel A. Jiménez and Ulrich Kremer, *Efficient Program Power Behavior Characterization*, Proceedings of the 2007 International Conference on High Performance Embedded Architectures & Compilers (HiPEAC-2007), pp. 183–197, January 2007. Acceptance rate: 29%.

Daniel A. Jiménez and Gabriel H. Loh, *Controlling the Power and Area of Neural Branch Predictors for Practical Implementation in High-Performance Processors*, Proceedings of the 18th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2006), pp. 55–62, October, 2006. Acceptance rate: 31%.

Miquel Pericàs, Adrian Cristal, Ruben González, Daniel A. Jiménez, and Mateo Valero, *A Decoupled Kilo-Instruction Processor*, Proceedings of the 12th International Symposium on High Performance Computer Architecture (HPCA-12), pp. 52-63, February, 2006. Acceptance rate: 15%.

Miquel Pericàs, Ruben González, Adrian Cristal, Daniel A. Jiménez, and Mateo Valero, *Chained In-Order/Out-of-Order DoubleCore Architecture*, Proceedings of the 17th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), pp 55-62, October 2005. Acceptance rate: 35%.

Miquel Pericàs, Adrian Cristal, Ruben González, Daniel A. Jiménez, and Mateo Valero, *Exploiting Execution Locality with a Decoupled Kilo-Instruction Processor*, Proceedings of the 6th International Symposium on High Performance Computing (ISHPC-VI), September 2005.

Daniel A. Jiménez, *Piecewise Linear Branch Prediction*, Proceedings of the 32nd International Symposium on Computer Architecture (ISCA-32), pp. 382-393, June 2005. Acceptance rate: 23%.

Daniel A. Jiménez, *Code Placement for Improving Dynamic Branch Prediction Accuracy*, Proceedings of the ACM SIGPLAN 2005 Conference on Programming Language Design and Implementation (PLDI), pp. 107–116, June, 2005. Acceptance rate: 21%.

Daniel A. Jiménez, *Fast Path-Based Neural Branch Prediction*, Proceedings of the 36th Annual International Symposium on Microarchitecture (MICRO-36), pp. 243–252, San Diego, CA, December 3-5, 2003. Acceptance rate: 26%.

Daniel A. Jiménez, *Reconsidering Complex Branch Predictors*, Proceedings of the Ninth International Symposium on High Performance Computer Architecture (HPCA-9), pp. 43–52, Anaheim, CA, February 2003. Acceptance rate: 22%.

Daniel A. Jiménez, Heather L. Hanson and Calvin Lin, *Boolean Formula-Based Branch Prediction for Future Technologies*, Proceedings of the International Conference on Parallel Architectures and Compilation Technologies (PACT), pp. 97–106, Barcelona, Spain 2001. Acceptance rate: 21%.

Daniel A. Jiménez and Calvin Lin, *Perceptron Learning for Predicting the Behavior of Conditional Branches* (**poster**), Proceedings of the 2001 INNS-IEEE International Joint Conference on Neural Networks (IJCNN), pp. 2122–2126, Washington, DC, 2001.

Daniel A. Jiménez and Calvin Lin, *Dynamic Branch Prediction with Perceptrons*, Proceedings of the 7th International Symposium on High Performance Computer Architecture (HPCA-7), pp. 197–206, Monterrey, Mexico, January 20-24, 2001. Acceptance rate: 24%.

Daniel A. Jiménez, Stephen W. Keckler and Calvin Lin, *The Impact of Delay on the Design of Branch Predictors*, Proceedings of the 33rd Annual International Symposium on Microarchitecture (MICRO-33), pp. 67–76, Monterey, California, December 10-13, 2000. Acceptance rate: 28%.

Daniel A. Jiménez and Nicolas Walsh, *Dynamically Weighted Ensemble Neural Networks for Classification*, Proceedings of the 1998 INNS-IEEE International Joint Conference on Neural Networks (IJCNN), pp. 753-756, Anchorage, Alaska 1998.

Daniel A. Jiménez, Tom Darm, Bill Rogers and Nicolas Walsh, *Locating Anatomical Landmarks for Prosthetics Design Using Ensemble Neural Networks*, Proceedings of the 1997 International Conference on Neural Networks (ICNN), volume 1, pp. 81–87., Houston, Texas, 1997.

Please note that in Computer Science systems research, top-tier conference publications rather than journal articles are the primary medium of academic discourse.

Journal Articles

Qixiao Liu, Miquel Moretó, Jaume Abella, Francisco J. Cazorla, Daniel A. Jiménez, and Mateo Valero, *Sensible Energy Accounting with Abstract Metering for Multicore Systems*, ACM Transactions on Architecture and Code Optimizations, Vol. 12 Issue 4, January 2016. *Paper was selected to appear at the HiPEAC 2016 conference*.

Zhe Wang*, Shuchang Shan, Ting Cao, Junli Gu, Yi Xu, Shuai Mu, Yuan Xie, Daniel A. Jiménez, *WADE: Writeback-Aware Dynamic Cache Management for NVM-based Main Memory System*, ACM Transactions on Architecture and Code Optimization, Vol. 10, No. 4, Article 51, Published December 2013. *Paper was selected to appear at the HiPEAC 2014 conference*.

Yingying Tian*, Samira M. Khan*, Daniel A. Jiménez, *Temporal-based Multi-level Correlating Inclusive Cache Replacement*, ACM Transactions on Architecture and Code Optimization, Vol. 10, No. 4, Article 33, Published December 2013. *Paper was selected to appear at the HiPEAC 2014 conference*.

Hyungjun Kim, Boris Grot, Paul V. Gratz, Daniel A. Jiménez, *Spatial Locality Speculation to Reduce Energy in Chip-Multiprocessor Networks-on-Chip*, Special Issue "NOCS Special Section," IEEE Transactions on Computers, Vol. 63, No. 3. March 2014.

Alaa R. Alameldeen, Nam Sung Kim, Samira M. Khan*, Hamid Reza Ghasemi, Chris Wilkerson, Jaydeep Kulkarni, and Daniel A. Jiménez, *Improving Memory Reliability, Power, and Performance using Mixed-Cell Designs*, Intel Technology Journal, Vol. 17, Issue 1, 2013 (reviewed internally by Intel technical staff).

Reena Panda, Paul Gratz, Daniel Jiménez, *B-Fetch:Branch Prediction Directed Prefetching for In-Order Processors*, IEEE Computer Architecture Letters, Vol. 11, No. 2, July-December 2012, IEEE Computer Society. **Selected to be presented in the "Best of CAL Session" at HPCA 2012**.

Renée St. Amant, Daniel A. Jiménez, and Doug Burger, *Mixed-Signal Approximate Computation: A Neural Predictor Case Study*, IEEE Micro, vol 29, no 1, "Top Picks from Computer Architecture Conferences," pp. 104–115, January/February 2009.

Daniel A. Jiménez, *Generalizing Neural Branch Prediction*, ACM Transactions on Architecture and Code Optimization, Vol. 5, No. 4, pp. 17:3–17:27, March 2009.

Chunling Hu*, Daniel A. Jiménez, Ulrich Kremer, *Combining Edge Vector and Event Counter for Time-dependent Power Behavior Characterization*, Transactions on High-Performance Embedded Architectures and Compilers II (Transactions on HiPEAC) Vol. 2, No. 1, LNCS Vol. 5470, pp. 85-104, 2009.

Miquel Pericàs, Adrian Cristal, Ruben González, Daniel A. Jiménez, and Mateo Valero, *Exploiting Execution Locality with a Decoupled Kilo-Instruction Processor*, Lecture Notes in Computer Science (subseries: Theoretical Computer Science and General Issues), Vol. 4759, pp. 56–67, 2008.

Gabriel Loh and Daniel A. Jiménez, *Modulo Path History for the Reduction of Pipeline Overheads in Path-Based Neural Branch Predictors*, International Journal of Parallel Programming (IJPP), Vol. 36, No. 2, pp. 267–286, April 2008.

Chunling Hu*, Daniel A. Jiménez, Ulrich Kremer, *An Evaluation Infrastructure for Power and Energy Optimizations*, International Journal of Embedded Systems (IJES) Vol. 3, No. 1/2, pp 31–42, 2007.

Daniel A. Jiménez, *Improved Latency and Accuracy for Neural Branch Prediction*, ACM Transactions on Computer Systems (TOCS), Vol. 23, No. 2, pp. 197–218, May 2005.

Daniel A. Jiménez, *Idealized Piecewise Linear Branch Prediction*, The Journal of Instruction-Level Parallelism (JILP), Vol. 7, April 2005.

Daniel A. Jiménez and Calvin Lin, *Neural Methods for Dynamic Branch Prediction*, ACM Transactions on Computer Systems (TOCS), Vol. 20, No. 4, pp. 369–397, November 2002.

Workshop Papers etc.

Yingying Tian*, Sooraj Puthoor, Joseph L. Greathouse, Bradford M. Beckmann and Daniel A. Jiménez, *Adaptive GPU Cache Bypassing*, Proceedings of the 8th Workshop on General Purpose Processing Using GPUs (GPGPU-8), pp. 25–35, (co-located with PPoPP 2015), San Francisco, CA, February 2015.

Daniel A. Jiménez, *Strided Sampling Hashed Perceptron Predictor*, The Journal of Instruction-Level Parallelism 4th JILP Workshop on Computer Architecture Competitions (JWAC-4), Championship Branch Prediction (CBP-4), (co-located with ISCA 2014), Minneapolis, Minnesota, June 2014.

Zhe Wang*, Samira M. Khan*, and Daniel A. Jiménez, *Rank Idle Time Prediction Driven Last-Level Cache Writeback*, Proceedings of the ACM SIGPLAN Workshop on Memory Systems Performance and Correctness (MSPC) (co-located with PLDI 2012), June 2012.

Zhe Wang* and Daniel A. Jiménez, *Exploiting Rank Idle Time for Scheduling Last-Level Cache Writeback*, (**poster and abstract for ACM Student Research Competition)**), Proceedings of the 2011 International Conference on Parallel Architectures and Compilation Technologies (PACT), Galveston, Texas, October 2011.

Yingying Tian* and Daniel A. Jiménez, *Sampling Temporal Touch Hint (STTH) Inclusive Cache Management Policy*, (**poster and abstract for ACM Student Research Competition)**), Proceedings of the 2011 International Conference on Parallel Architectures and Compilation Technologies (PACT), Galveston, Texas, October 2011.

Samira M. Khan* and Daniel A. Jiménez, *Decoupled Cache Segmentation: Mutable Policy with Automated Bypass*, (**poster and abstract for ACM Student Research Competition)**), Proceedings of the 2011 International Conference on Parallel Architectures and Compilation Technologies (PACT), Galveston, Texas, October 2011.

Daniel A. Jiménez, *OH-SNAP: Optimized Hybrid Scaled Neural Analog Predictor*, 2nd JILP Workshop on Computer Architecture Competitions (JWAC-2) (co-located with ISCA 2011), San Jose, California, June 2011.

Daniel A. Jiménez, *SNIP: Scaled Neural Indirect Predictor*, 2nd JILP Workshop on Computer Architecture Competitions (JWAC-2) (co-located with ISCA 2011), San Jose, California, June 2011.

Zhe Wang*, Daniel A. Jiménez, *Understanding Performance using Code Reordering*, Poster session of the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS Poster), Pittsburgh, PA, March 2010.

Yingying Tian*, Samira Khan*, Daniel A. Jiménez, *Using Pattern Sampling to Simplify and Improve L2 Caches*, Poster session of the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS Poster), Pittsburgh, PA, March 2010.

Samira Khan*, Daniel A. Jiménez, Doug Burger and Babak Falsafi, *Using Dead Blocks as a Virtual Victim Cache*, Proceedings of the 2010 4th Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI), co-located with HPCA-2010, January 2010.

Shah Mohammad Faizur Rahman*, Zhe Wang*, and Daniel A. Jiménez, *Studying Microarchitectural Structures with Object Code Reordering*, Proceedings of the 2009 Workshop on Binary Instrumentation and Applications (WBIA), December, 2009.

Samira Khan*, Daniel A. Jiménez, Doug Burger and Babak Falsafi, *Using Dead Blocks as a Virtual Victim Cache*, Poster session of the International Conference on Architectural Support for

Programming Languages and Operating Systems (ASPLOS Poster), Washington, D.C., March 2009.

Daniel A. Jiménez, *The Subconcious Mind of a Branch Predictor*, Wild and Crazy Ideas VI (WACI-VI) (co-located with ASPLOS XII), Seattle, Washington, March 2008.

Chunling Hu*, John McCabe*, Daniel A. Jiménez and Ulrich Kremer, *Infrequent Basic Block-based Program Phase Classification and Power Behavior Characterization*, Proceedings of the 10th IEEE Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-2006), pp. 34–43, February, 2006.

Chunling Hu*, John McCabe*, Daniel A. Jiménez and Ulrich Kremer, *The Camino Compiler Infrastructure*, Proceedings of the 2005 Workshop on Binary Instrumentation and Applications (WBIA), pp. 7–12, September, 2005.

Gabriel H. Loh and Daniel A. Jiménez, *Reducing the Power and Complexity of Path-Based Neural Branch Prediction*, Proceedings of the 2005 Workshop on Complexity-Effective Design (WCED'05), June, 2005.

Chunling Hu*, Daniel A. Jiménez and Ulrich Kremer, *Toward an Evaluation Infrastructure for Power and Energy Optimizations*, Proceedings of the First Workshop on High-Performance, Power-Aware Computing (HP-PAC 2005) (co-located with IPDPS 2005), April 2005.

Daniel A. Jiménez, *Idealized Piecewise Linear Branch Prediction*, The First JILP Championship Branch Prediction Competition (CBP-1) (co-located with MICRO-37), December 2004.

Ravi Batchu* and Daniel A. Jiménez, *Exploiting Procedure Level Locality to Reduce Instruction Cache Misses*, Proceedings of the 8th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-8), Madrid, Spain, pp 75–84, February 15, 2004.

Daniel A. Jiménez and Calvin Lin, *Branch Path Re-Aliasing*, Proceedings of the 4th Workshop on Feedback Directed and Dynamic Optimization (FDDO-4), Austin, TX, pp. 83–92, December 2001.

Other Publications

Ravi Batchu* and Daniel A. Jiménez, *Exploiting Procedure Level Locality to Reduce TLB Overhead*, DCS-TR-XXX, Department of Computer Science, Rutgers University, May 2004 (TR number pending).

Ravi Batchu* and Daniel A. Jiménez, *Exploiting Procedure Level Locality to Reduce Instruction Cache Misses*, technical report DCS-TR-532, Department of Computer Science, Rutgers University, July, 2003.

Nitya Ranganathan, Ramadass Nagarajan, Daniel Jiménez, Doug Burger, Stephen W. Keckler, and Calvin Lin, *Combining Exit Prediction and Hyperblocks to Improve Front-End Bandwidth and Performance*, technical report TR-02-41, Department of Computer Sciences, The University of Texas at Austin, September 2002.

Samuel Z. Guyer, Daniel A. Jiménez, and Calvin Lin, *The C-Breeze Compiler Infrastructure*, technical report TR-01-43, Department of Computer Sciences, The University of Texas at Austin, 2001.

Daniel A. Jiménez, *Delay-Sensitive Branch Predictors for Future Technologies*, Doctoral dissertation, Department of Computer Sciences, The University of Texas at Austin, 2001.

Daniel A. Jiménez, Tom Darm, Bill Rogers and Nicolas Walsh, *A Method for Locating BK Anatomical Landmarks for a Laser Scanning Imager* (invited paper), Proceedings of the International Symposium on CAD/CAM Systems in Pedorthics, Prosthetics and Orthotics, Nürnberg, Germany, 1997.

Daniel A. Jiménez, *Methods for Satisfying Hard Boolean Formulas*, Master's thesis, Division of Mathematics, Computer Science, and Statistics, The University of Texas at San Antonio, May

1994.

Alex López-Ortiz, Daniel A. Jiménez, *Comp.Theory FAQ*, a frequently-asked questions (FAQ) list for the Usenet newsgroup **comp.theory**, at
http://db.uwaterloo.ca/~ alopez-o/comp-faq/faq.html

Daniel A. Jiménez, *Program a RAM Disk*, Rainbow: The Color Computer Monthly Magazine, January, 1989.

Grants/Gifts

NSF CCF-1649242, "EAGER: Deep Learning for Microarchitectural Prediction," $150,000, awarded August 1, 2016, expires July 31, 2018 (PI).

Intel Corporation, "Coordinated Memory Hierarchy Management and Speculation for Emerging Memory Technologies," $225,000, January 2016, (co-PI; PI is Paul Gratz at TAMU).

Intel Corporation, "Developing an Open-Source Trace-Based Microarchitecture Simulator," $30,000, agreed on July 10, 2014, pending transfer of funds.

NSF CCF-1162215, "SHF: Medium: Title: Idempotent Processing and Architectures" $600,000. Jiménez is the PI at TAMU, Karu Sankaralingam is the PI at Wisconsin. Jiménez's portion is $150,000, awarded August 1, 2012, expires January 31, 2017.

NSF CCF-1216604/1332598, "SHF:CSR:Small:Improving Processor Efficiency with Prediction," $350,000, awarded July 2012, expires July 2017 (PI).

NSF DUE-1027521, "Scholarship for Service - The University of Texas at San Antonio," $1,333,658 effective January 2011, expires August 2015 (co-PI) (Jiménez is still co-PI as of this writing but his role is minimal since moving to TAMU).

Intel Corporation, "Prediction for Memory Hierarchy and Processor Core Optimization," $5,000 effective September 2011 (PI).

NSF CCF-1012127/1332654, "SHF: Large: Collaborative Research: Reliable Performance for Modern Systems," $550,000. Jiménez is the PI at TAMU, Emery Berger is the PI at UMass. Jiménez's portion is $203,750, awarded July 2010, expired July 2014.

NHARP-010115-0079-2009, "Improving Multi-Core Processor Efficiency by Reducing Memory System Waste," $150,000, awarded August 2010, expired April 2013 (PI).

NSF CCF-0952604, "EAGER: Code-Improving Transformations for Branch Prediction," $100,000, awarded September, 2009, expired February 2012 (PI).

NSF CCF-0829760, "Systems Research Mentoring Workshop," $25,000, awarded April 2008, expired April 2010 (co-PI).

NSF CNS-0751138, "CRI:IAD Resources for Branch Prediction Research," $233,730, awarded June 2008, expired May 2010 (PI).

NSF CCF-0545898/0931874/1332597, "CAREER: Branch Prediction," $400,000, awarded April 2006, expired March 2014 (PI).

Ministerio de Educación y Ciencia (Spanish Ministry of Education and Science) SB2003-0357, "Ayudas para movilidad de Profesores de Universidad e Investigadores españoles y extranjeros" (Mobility assistance for Spanish and foreign university professors and researchers), with Mateo Valero, approved as of August 2004.

NSF CSA-0311091, "Improving Microarchitectural Performance with Neural Predictors," $224,916, awarded July 2003, expired 2006 (PI).

Rutgers Information Sciences and Technology Council, "An Evaluation Infrastructure for Power and Energy Optimizations," with Ulrich Kremer, $30,294, awarded May 2003, expired April 2004 (co-PI).

Invited Talks (selected)

Insertion and Promotion for Tree-Based PseudoLRU Last-Level Caches, January 2014, invited talk at the University of Texas at San Antonio.

Improving Last-Level Cache Replacement, June 2013, invited talk at the Technical University of Catalonia (UPC).

What is the Goal of Computer Architecture Research?, February 2012, **keynote presentation**, The 7th International Workshop on Unique Chips and Systems (UCAS-7), co-located with HPCA 2012.

An Optimized Scaled Neural Branch Predictor, invited talk, Texas A&M University, October 2011.

Reducing Wasted Speculation, invited talk, University of Massachusetts Amherst, December 2010.

Reducing Wasted Speculation, October 2010, invited talk at the Technical University of Catalonia (UPC).

Studying Microarchitectural Structures with Object Code Reordering, December 2009, invited talk at the Technical University of Catalonia (UPC).

Low-Power, High-Performance Analog Neural Branch Prediction, invited talk, High-Performance Computing Group Seminar, Department of Computer Architecture Technical University of Catalonia (UPC), December 2008.

Improving Performance with Neural Branch Prediction, invited talk, Department of Computer Science, The University of Texas at Brownsville, November 2008.

Efficient Power Behavior Characterization, High-Performance Computing Group Seminar, Department of Computer Architecture, Technical University of Catalonia (UPC), Barcelona, Spain, May 2007.

Recent Advances in Branch Prediction, TU Delft, May 2006, Ghent University, May 2006, Technical University of Barcelona, May 2006, University Complutense of Madrid, May 2007, University of Edinburgh, May 2007.

Code Placement for Improving Dynamic Branch Prediction Accuracy, Intel Microprocessor Research Laboratory, Barcelona, Spain, August 2005.

Idealized Piecewise Linear Branch Prediction, High-Performance Computing Group Seminar, Department of Computer Architecture, Technical University of Catalonia (UPC), Barcelona, Spain, February 2005.

Perceptrons for Dummies, The First JILP Championship Branch Prediction Competition (CBP-1) (co-located with MICRO-37), Portland, Oregon, December 2004.

Dynamic Branch Prediction with Perceptrons, at Research, Careers, and Computer Science: A Maryland Symposium, Department of Computer Science, The University of Maryland, College Park, Maryland, November 2001.

Delay Sensitive Branch Predictors, Dept. de Arquitectura de Computadores, Universidad Politecnica de Catalunya, Barcelona, Spain, September 2001.

A Method for Locating BK Anatomical Landmarks for a Laser Scanning Imager, at the International Symposium on CAD/CAM Systems in Pedorthics, Prosthetics and Orthotics, Nürnberg, Germany, 1997.

Selected Presentations

An Optimized Scaled Neural Branch Predictor, The 2011 IEEE International Conference on Computer Design (ICCD), Amherst, Massachusetts, October, 2011.

Insertion Policy Selection Using Decision Tree Analysis, The 2010 IEEE International Conference on Computer Design (ICCD), Amsterdam, Netherlands, October, 2010.

Using Dead Blocks as a Virtual Victim Cache, 2010 4th Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI), co-located with HPCA-2010, January 2010.

Studying Microarchitectural Structures with Object Code Reordering, 2009 Workshop on Binary Instrumentation and Applications (WBIA), December, 2009.

Composite Confidence Estimators for Enhanced Speculation Control, The 21st International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2009), Sao Paulo, Brazil, October, 2009.

Piecewise Linear Branch Prediction, The 32nd International Symposium on Computer Architecture (ISCA-32), Chicago, Illinois, June 2005.

Code Placement for Improving Dynamic Branch Prediction Accuracy, The ACM SIGPLAN 2005 Conference on Programming Language Design and Implementation (PLDI), Madison, Wisconsin, 2005.

Idealized Piecewise Linear Branch Prediction, The First JILP Championship Branch Prediction Competition (CBP-1) (co-located with MICRO-37), Portland, Oregon, December 2004.

Exploiting Procedure Level Locality to Reduce Instruction Cache Misses, at the 8th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-8), Madrid, Spain, February 15, 2004.

Fast Path-Based Neural Branch Prediction, at the 36th International Symposium on Microarchitecture (MICRO-36), San Diego, California, December 2003.

Reconsidering Complex Branch Predictors, at the 9th International Symposium on High Performance Computer Architecture (HPCA-9), Anaheim, California, February 2003.

Neural Methods for Dynamic Branch Prediction, at the Annual Current DCS Research Seminar, Rutgers University, November, 2002.

Branch Path Re-Aliasing, at the 4th Workshop on Feedback Directed and Dynamic Optimization (FDDO-4) (co-located with MICRO-34), December, 2001

Boolean Formula-based Branch Prediction for Future Technologies, at the International Conference on Parallel Architectures and Compilation Technologies (PACT), Barcelona, Spain, September 2001.

Dynamic Branch Prediction with Perceptrons, at the 7th International Symposium on High Performance Computer Architecture (HPCA-7), Monterrey, Mexico, January, 2001.

The Impact of Delay on the Design of Branch Predictors, at the 33rd Annual International Symposium on Microarchitecture (MICRO-33), Monterey, California, December, 2000.

Locating Anatomical Landmarks for Prosthetics Design using Ensemble Neural Networks, at the International Conference on Neural Networks (ICNN), Houston, Texas, 1997.

Dynamically Weighted Ensemble Neural Networks for Classification, at the 1998 INNS-IEEE International Joint Conference on Neural Networks (IJCNN), Anchorage, Alaska 1998.

University Leadership

Caucus Leader, Engineering Caucus of the Faculty Senate, Texas A&M College of Engineering (2016-present).

Chair, Texas A&M Department of Computer Science and Engineering Admissions Graduate Advisory Committee (2016-present).

Chair, Texas A&M Department of Computer Science and Engineering Admissions Committee Subcommittee on Graduate Recruitment (2014-present).

Chair, Texas A&M Department of Computer Science and Engineering Research Computing Services Commitee (2013-2015)

Department Chair, UT San Antonio Department of Computer Science (2011-2012)

Chair, UT San Antonio Department of Computer Science Junior Faculty Mentoring Task Force (2010)

University Service

Member, Texas A&M University Core Curriculum Council (2015-present)

Member, Texas A&M University Council of Principal Investigators (2013-2014, 2015-2017)

Member, Texas A&M Department of Computer Science and Engineering Advisory Committee (2014-present).

Senator, Texas A&M Faculty Senate (2013-2016).

Member (Faculty Senate Representative), Texas A&M University Email Selection Committee (2013-present)

Member, Texas A&M Department of Computer Science and Engineering Graduate Advisory Committee (2013-2015)

Member, Texas A&M Department of Computer Science and Engineering Climate Committee (2013-present)

Member, Texas A&M College of Engineering Honors and Awards Committee (2013-2015)

Member, UT San Antonio Social Networking Task Force 2011

Senator, UT San Antonio Faculty Senate (2010-2012)

Member, UT San Antonio Department of Computer Science Curriculum Sub-Committee on CS 1063

Member, UT San Antonio Department of Computer Science Periodic Performance Evaluation Committee, 2008

Member, UT San Antonio Faculty Recruiting Committee, 2008-present

Member, UT San Antonio Graduate Studies Committee, 2008-2009

Member, UT San Antonio Department of Computer Science Curriculum Committee, 2007-2008

Member, UT San Antonio College of Sciences College Faculty Review Advisory Committee, 2008-present

Member, UT San Antonio Department of Computer Science Departmental Faculty Review Advisory Committee, 2007-present

Member, Rutgers DCS Graduate Admissions Committee, 2003

Member, Rutgers DCS Graduate Admissions Committee, 2004

Member, Rutgers DCS Graduate Program Committee, 2005-2006

Teaching (at Rutgers)

CS 673 - Readings in Instruction-Level Parallelism, Spring 2003.

CS 507 - Advanced Computer Architecture, Fall 2006.

CS 505 - Computer Structures, Fall 2002, Fall 2003, Fall 2004, Spring 2006.

CS 211 - Computer Architecture, Spring 2004, Fall 2005, Spring 2006.

CS 500 - Light Seminar: Machine Learning in Computer Architecture and Compilers, Fall 2004.

Teaching (at UTSA)

CS 1073 - Introductory Computer Programming for Scientific Applications, Fall 1996.

CS 1713 - Introduction to Computer Science, Spring 1997, Summer 1997, Fall 1997.

CS 1713 - Introduction to Computer Programming II, Spring 2009, Spring 2011.

CS 1723 - Data Structures, Spring 1994, Summer 1998.

CS 2073 - Computer Programming with Engineering Applications, Fall 1992, Spring 1993, Fall 1997, Spring 2007, Spring 2009.

CS 2083 - Microcomputer Applications, Fall 1993, Spring 1994.

CS 2733 - Computer Organization II, Fall 2007.

CS 2743 - Data Structures II, Spring 1993.

CS 3343 - Analysis of Algorithms, Spring 1998, Summer 2007.

CS 3843 - Computer Organization, Fall 2008, Spring 2011.

CS 3853 - Computer Architecture, Fall 2009, Spring 2010.

CS 5513 - Computer Architecture, Fall 2007, Fall 2008, Fall 2009, Fall 2011.

CS 6513 - Advanced Architecture, Spring 2012.

Teaching (at TAMU)

CSCE 689 - Microarchitecture (Spring 2013).

CSCE 689 - Architectural Support for Programming Languages and Operating Systems (Fall 2013).

CSCE 614 - Computer Architecture (Spring 2014, Fall 2015)

CSCE 689 - Fundemental Concepts in Computer Science (Fall 2014)

CSCE 613 - Advanced Operating Systems (Spring 2015)

Students Supervised

Sangam Jindal, dissertation title to be decided, Ph.D., graduation expected 2019

Samira Mirbagher, “Branch Prediction Techniques,” Ph.D., graduation expected 2019

Roger Brewer, REU student from Purdue at TAMU, “Managing a Die-stacked DRAM Cache,” Summer 2014

Elvira Teran, Ph.D., “Principled Approaches to Last-Level Cache Management,” **graduated with Ph.D.** from Texas A&M, Summer 2017.

Yingying Tian, Ph.D., “Reducing Waste in Memory Hierarchies,” **graduated with Ph.D.** from Texas A&M, Fall 2015.

Zhe Wang, Ph.D., “Improving Processor Design by Exploiting Program Variance,” **graduated with Ph.D.** from Texas A&M Summer 2014.

Samira M. Khan, Ph.D. “Intelligent Cache Management Techniques,” **graduated with Ph.D.** from UTSA, Spring 2011.

Chunling Hu, Ph.D. “An Infrastructure for Program Power Behavior Characterization and Optimization Evaluation,” **graduated with Ph.D.** from Rutgers, Summer 2007.

Abhishek Mehrotra, “Optimizing on-chip memory allocation to maximize performance,” Rutgers Master’s Essay completed Spring 2004.

Kris Rutkowski, “Branch Prediction for Sorting Algorithms,” Rutgers Master’s Essay completed Spring 2004.

Charles Ganansia, “Fast Binary Addition,” Rutgers Master’s Essay completed Spring 2004.

Ravi V. Batchu, Ph.D., “Temporal Locality at Procedure Level – Its Study and Exploitation,” **graduated with Ph.D.** from Rutgers, Fall 2003

Timothy Munar, “Hardware Implementation of Data Prefetching,” Rutgers Master’s Essay completed Spring 2003.

Peng Zhou, “Performance from Hardware: Different Choices of Microarchitectural CPU Parameters,” Rutgers Master’s Essay completed Spring 2003.

Other Graduate Student Committees

Renée St. Amant, “Mixed-Signal Microarchitecture Design for Energy-efficient, Approximate Computing,” doctoral dissertation committee, University of Texas at Austin (supervising professor Doug Burger), defense scheduled for April 2014.

Nityendra Singh Master’s thesis committee, Texas A&M University, (supervising professor Peng Li), expected May 2014.

Prabal Sharma “A Branch-directed Data Cache Prefetcher For Out-of-Order Processors,” Master’s thesis committee, Texas A&M University, (supervising professor Paul Gratz), defended June 2013.

Hyungjun Kim, “Energy and Reliability in Future NOC Interconnected CMPs,” doctoral dissertation committee, Texas A&M University, (supervising professor Paul Gratz), defended June 2013.

Muhammad Umar Farooq, “Addressing Control-Flow Bottlenecks Using Compiler Guided Techniques,” doctoral dissertation committee, University of Texas at Austin, (supervising professor Lizy John), defended March 2013.

Nitya Ranganathan, “Control Flow Speculation for Distributed Architectures,” doctoral dissertation committee, University of Texas at Austin, (supervising professor Doug Burger), defended Fall 2008.

Veerle Desmet, “On the Systematic Design of Cost-Effective Branch Prediction,” doctoral dissertation committee, Ghent University, Belgium, (supervising professor Koen De Bosschere), defended Spring 2006.

Lei Wang, “Optimally Balanced Forward Degree Sequence,” Rutgers doctoral qualifying exam, (supervising professor Mario Szegedy), completed Spring 2006.

Chen Fu, “Testing of Java Web Services for Robustness,” Rutgers doctoral qualifying exam, (supervising professor Barbara Ryder), Spring 2004.

Xiaoyan Li, “Using Adaptive Range Control to Optimize 1-hop Broadcast Coverage in Dense Wireless Sensor Networks,” Rutgers doctoral qualifying exam, (supervising professor Richard Martin), Summer 2003.

Eduardo Pinheiro, Rutgers doctoral qualifying exam, (supervising professor Ricardo Bianchini), “Power and Energy Conservation for Clusters,” Fall 2002.

Professional Activities - Leadership

Executive Committee Member, IEEE Technical Committee on Computer Architecture (TCCA), 2015 – present

Program Chair, 23rd IEEE International Symposium on High-Performance Computer Architecture (HPCA-2017).

General Chair, 17th IEEE International Symposium on High-Performance Computer Architecture (HPCA-2011).

Organizer, CRA-W/CDC Distinguished Lecture Series event at UT San Antonio: “Doctoral Studies in Computing,” March 2010

Moderator and Presenter, UTSA College of Sciences Research Conference, August 2009

Co-Chair, CRA-W/CDC Mentoring Workshop for Systems Research, The University of Delaware, June 2008.

Guest Editor, Journal of Instruction-Level Parallelism (JILP), 2007.

Co-Chair, CRA-W/CDC Programming Languages Summer School, The University of Texas at Austin, May 2007.

Chair, 2nd Championship Branch Prediction Workshop (CBP-2006).

Professional Activities - Committees

Program Committee Member, IEEE Micro “Top Picks from the Computer Architecture Conferences” (Top Picks 2017).

Program Committee Member, 45th International Symposium on Computer Architecture (ISCA 2018)

Program Committee Member, 24th International Symposium on High-Performance Computer Architecture (HPCA-2018).

Program Committee Member, 50th International Symposium on Microarchitecture (MICRO 2017)

Program Committee Member, 2nd Cache Replacement Competition (CRC2 2017)

Program Committee Member, ACM International Conference on Supercomputing (ICS-2017).

Extended Program Committee Member, 44th International Symposium on Computer Architecture (ISCA 2017)

Program Committee Member, 25th International Conference on Parallel Architectures and Compilation Techniques (PACT-2016)

Program Committee Member, 43rd International Symposium on Computer Architecture (ISCA 2016)

Program Committee Member, 9th Workshop on General Purpose Processing Using GPUs, 2016 (GPGPU-9)

Program Committee Member, 2016 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2016)

Member, External Review Committee, 24th International Symposium on High-Performance Computer Architecture (HPCA-2016).

Program Committee Member, 48th International Symposium on Microarchitecture (MICRO 2015)

Program Committee Member, 2nd Data Prefetching Championship (DPC2 2015)

Publicity Chair, International Conference on High Performance Embedded Architectures and Compilers (HiPEAC 2016)

External Review Committee Member, 42nd International Symposium on Computer Architecture (ISCA-2015)

Member, External Review Committee, 23rd International Symposium on High-Performance Computer Architecture (HPCA-2015).

Member, External Review Committee, 47th International Symposium on Microarchitecture (MICRO-2014).

Member, Board of Distinguished Reviewers, ACM Transactions on Architecture and Code Optimization, 2014

Program Committee Member, ACM International Conference on Supercomputing (ICS-2014).

Program Committee Member, IEEE Micro "Top Picks from the Computer Architecture Conferences" (Top Picks 2014).

Member, Board of Distinguished Reviewers, ACM Transactions on Architecture and Code Optimization, 2013

Program Committee Member, 45th International Symposium on Microarchitecture (MICRO-2012).

Steering Committee Member, 20th International Symposium on High-Performance Computer Architecture (HPCA-2013).

Steering Committee Member, 19th International Symposium on High-Performance Computer Architecture (HPCA-2012).

Program Committee Member, JILP Workshop on Computer Architecture Competitions: Championship Branch Prediction (JWAC-2) 2011.

Program Committee Member, 17th International Symposium on High-Performance Computer Architecture (HPCA-2011).

Program Committee Member, 38th International Conference on Parallel Processing (ICPP-2009).

Program Committee Member, 21st ACM International Conference on Supercomputing (ICS-2007).

Program Committee Member, 20th ACM International Conference on Supercomputing (ICS-2006).

Program Committee Member, 33rd International Symposium on Computer Architecture (ISCA-2006).

Program Committee Member, 38th International Symposium on Microarchitecture (MICRO-2005).

Publications Chair, 37th International Symposium on Microarchitecture (MICRO-2004).

Program Committee Member, 14th International Symposium on Parallel Architectures and Compilation Techniques (PACT-2005).

Program Committee Member, 13th International Symposium on Parallel Architectures and Compilation Techniques (PACT-2004).

Program Committee Member, 10th International Conference on High Performance Computing (HiPC-2003).

Professional Activities - Panels

Panelist, NSF [program name redacted], 2014 (December).

Panelist, NSF [program name redacted], 2014 (April).

Panelist, NSF [program name redacted], 2013 (May).

Panelist, NSF [program name redacted], 2013 (April).

Distinguished Speaker, CRA-W/CDC Distinguished Lecture at University of Texas at El Paso / New Mexico State University, 2013

Panelist, Academic Workshop for Underrepresented Ethnic Minorities and People with Disabilities at the level of Assistant Professor, Associate Professor, and Senior Doctoral Student, 2011

Panelist, NSF [program name redacted], 2009.

Presenter, CRA-W/CDC Careers in High Performance Systems (CHiPS) Mentoring Workshop, NCSA, Urbana-Champaign, Illinois, July 2009.

Presenter, PLOSA 2009: CRA-W/CDC Programming Languages, Operating Systems, & Architecture Workshop, Washington D.C., March 2009.

Panelist, NSF [program name redacted], 2007.

Professional Activities - Reviewing

Reviewer, 41st International Symposium on Computer Architecture (ISCA-2014).

Reviewer, 20th International Symposium on High-Performance Computer Architecture (HPCA-2014).

Reviewer, 39th ACM/IEEE International Symposium on Computer Architecture (ISCA-2012).

Reviewer, 18th International Symposium on High-Performance Computer Architecture (HPCA-2012).

Reviewer, ACM Transactions on Architecture and Code Optimization (ACM TACO), 2011.

Reviewer, 44th International IEEE/ACM Symposium on Microarchitecture (MICRO-2011).

Reviewer, 15th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2009.

Reviewer, 41st International Symposium on Microarchitecture (MICRO-2008).

Reviewer, 15th International Symposium on High-Performance Computer Architecture (HPCA-2008).

Reviewer, 22nd ACM International Conference on Supercomputing (ICS-2008).

Reviewer, ACM SIGPLAN 2008 Conference on Programming Language Design and Implementation (PLDI).

Reviewer, 2008 International Symposium on Code Generation and Optimization (CGO).

Reviewer, 13th International Symposium on High-Performance Computer Architecture (HPCA-2007).

Reviewer, 39th International Symposium on Microarchitecture (MICRO-2006).

Reviewer, Journal of Systems Architecture (JSA), 2006.

Reviewer, 12th International Symposium on High-Performance Computer Architecture (HPCA-2006).

Reviewer, Journal of Machine Learning Research, 2005.

Reviewer, 2005 International Conference on High Performance Embedded Architectures and Compilers (HiPEAC 2005).

Reviewer, ACM Transactions on Architecture and Code Optimization (ACM TACO), 2005.

Reviewer, 12th International Conference on High Performance Computing (HiPC-2005).

Reviewer, 32nd International Symposium on Computer Architecture (ISCA-2005).

Reviewer, 2005 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS).

Reviewer, 11th International Symposium on High-Performance Computer Architecture (HPCA-2005).

Reviewer, ACM SIGPLAN 2004 Conference on Programming Language Design and Implementation (PLDI).

Reviewer, 31th International Symposium on Computer Architecture (ISCA-2004).

Reviewer, Journal of Instruction-Level Parallelism (JILP), 2004.

Reviewer, 2004 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS).

Reviewer, 12th International Symposium on Parallel Architectures and Compilation Techniques (PACT-2003).

Reviewer, IEEE Transactions on Computers, 2003, 2008.

Reviewer, 36th International Symposium on Microarchitecture (MICRO-2003).

Reviewer, 30th International Symposium on Computer Architecture (ISCA-2003).

Reviewer, 2003 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS).

Reviewer, Journal of Instruction-Level Parallelism (JILP), 2003.

Reviewer, 29th International Symposium on Computer Architecture (ISCA-2002).

Reviewer, 10th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS).

Reviewer, 34th International Symposium on Microarchitecture (MICRO-2001).

Reviewer, 10th International Symposium on Parallel Architectures and Compilation Techniques (PACT-2001).

Reviewer, 2001 European Conference on Parallel Computing (EUROPAR).

Reviewer, IEE Proceedings on Computers and Digital Techniques

Reviewer, Journal of Parallel and Distributed Computing (JPDC).

Reviewer, Archives of Physical Medicine and Rehabilitation.

Professional Activities - Miscellaneous

Member of the Association for Computing Machinery, 1999 - present

Member of IEEE and IEEE Computer Society, 2002 - present

Assistant Instructor, University of Texas WTF Taekwondo Club, 2000 - 2002

November 29, 2017